Kyle Woodworth

Superconducting Electronics Design Engineer

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EDUCATION

University of Wisconsin-Madison, Madison, WI — 2025-Present
Ph.D. in Electrical Engineering

Purdue University, West Lafayette, IN — 2015-2017
M.S. in Electrical Engineering

Purdue University, West Lafayette, IN — 2011-2015
B.S. in Electrical Engineering

PROFESSIONAL EXPERIENCE

Fermilab, Batavia, IL — Aug 2021 - Present
ASIC Design Engineer

- Designed and tested ion-trap control electronics for the CITC and ACC programs, including development of a precision charge-integrating DAC architecture for stable, low-noise electrode biasing and waveform generation.
- Contributed to the design and analysis of superconducting parametric amplifiers, supporting low-noise readout chains for cryogenic detector and quantum measurement systems.
- Designed and validated a high-speed SLVS interface implemented in a 28 nm CMOS process, including simulation, verification, and lab testing to ensure signal integrity and reliable high-throughput data transfer.

Northrop Grumman Corporation, Baltimore, MD — July 2018 - Aug 2021
Superconducting Electronics Design Engineer

- Modeled and verified superconducting systems using SystemVerilog, Verilog-AMS, and SPICE.
- Designed and verified systems/components with Cadence, Mentor Graphics, and HFSS.
- Developed SKILL automation and parameterized cells to improve superconducting design flow.

Northrop Grumman Corporation, Baltimore, MD — May 2017 - Aug 2017
Superconducting Electronics Design Automation Intern

- Contributed to early development work related to reciprocal quantum logic.

Northrop Grumman Corporation, Baltimore, MD — May 2016 - Aug 2016
Process Design Kit Engineering Intern

- Integrated and compared Cadence PPC and Mentor Graphics OPC flows for internal technologies.

Micron Technology, Boise, ID — May 2015 - Aug 2015
Enterprise Firmware Test Engineering Intern

- Ported an internal Windows NVMe test platform and associated tools into a Linux environment.
- Tools: Linux kernel, NVMe drives, JTAG, Python, C/C++, Git/SVN.

Micron Technology, Boise, ID — May 2014 - Aug 2014
Enterprise Firmware Test Engineering Intern

- Automated SCSI trace analysis using the provided analyzer API to reduce manual inspection effort.
- Tools: C/C++, Python, SCSI analyzer, NVMe drives, Linux, Git/SVN.

Intel Corporation, Folsom, CA — Jan 2013 - May 2013
Design Automation Engineering Intern

- Designed an internal website to present design environment states and shared resources.
- Tools: Microsoft SharePoint, Cadence, Perl, Bash, HTML/PHP/JavaScript.

RESEARCH

University of Wisconsin-Madison, Madison, WI — Fall 2025-Present
Ph.D. Researcher

- Simulating and modeling electromagnetic trapped flux behavior in superconducting circuits.

Purdue University, West Lafayette, IN — Spring 2017
Graduate Researcher

- Set up PDK and design environment for MITLL 90nm process to support undergraduate SoC research.
- Designed, simulated, and verified CFlash memory cells for 45nm-node evaluation.
- Developed layout and automated generation flow for an integrated triple-cascode transistor array for mm-wave amplifier work.

TEACHING

Purdue University, West Lafayette, IN — 2016-2017
Graduate Teaching Assistant, ECE49595 - Senior Design

- Advised senior capstone teams from design specification through PCB prototyping.

AWARDS & CO-CURRICULARS

Purdue System-on-Chip Team — 2016
Team Leader, Bootstrapping

Purdue University ECE Student Society — 2015-2016
Academic Chair

Purdue System-on-Chip Team — 2014-2015
Team Member

Purdue University Spark Challenge — 2011-2015
Staff

Sons of the American Legion Scholarship — 2011-2015

SKILLS

Design & Modeling
Cadence, Mentor Graphics, HFSS, SPICE, Verilog-AMS, SystemVerilog

Programming & Automation
Python, C/C++, Bash, SKILL, Perl, Rust

Systems & Tooling
Linux, Git/SVN, JTAG, Oscilloscopes, Power Supplies, Spectrum Analyzers